

FIG. 1A

FIG. 1B

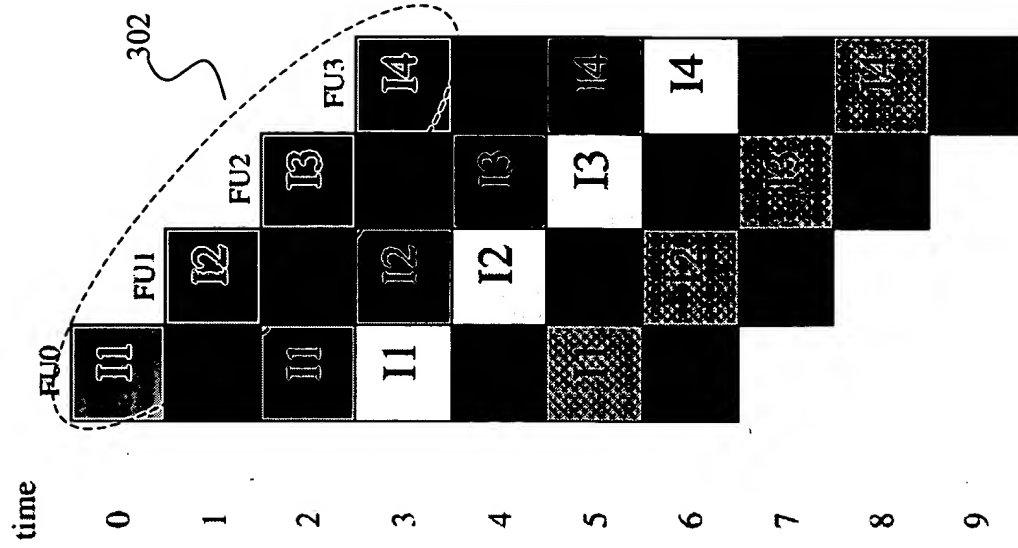


FIG. 2

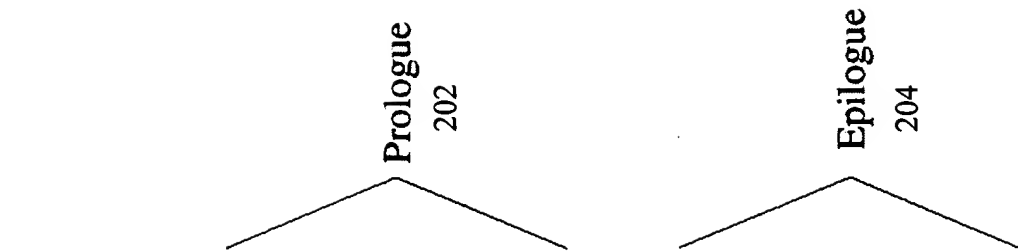


FIG. 3

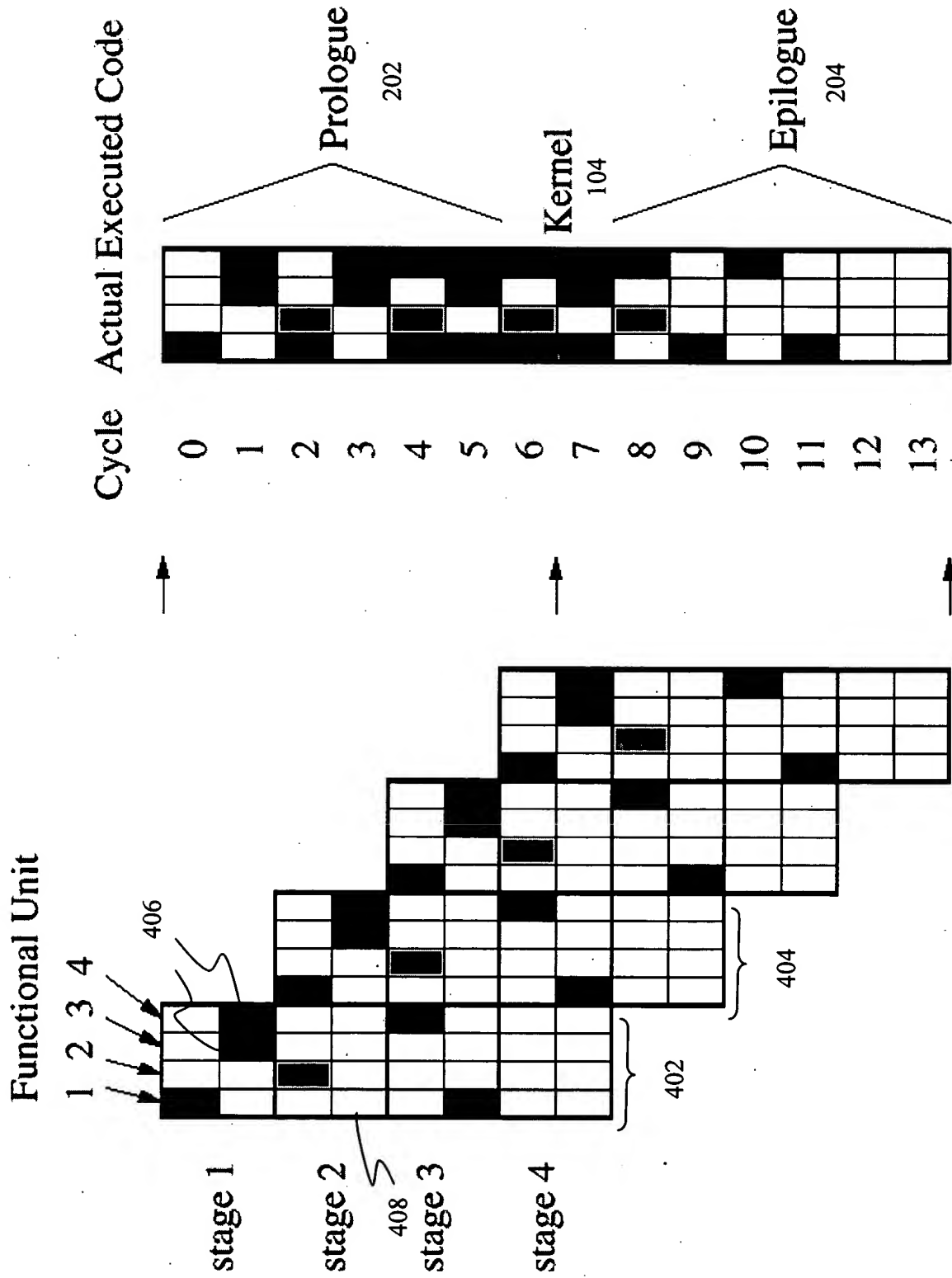


FIG. 4A

FIG. 4B

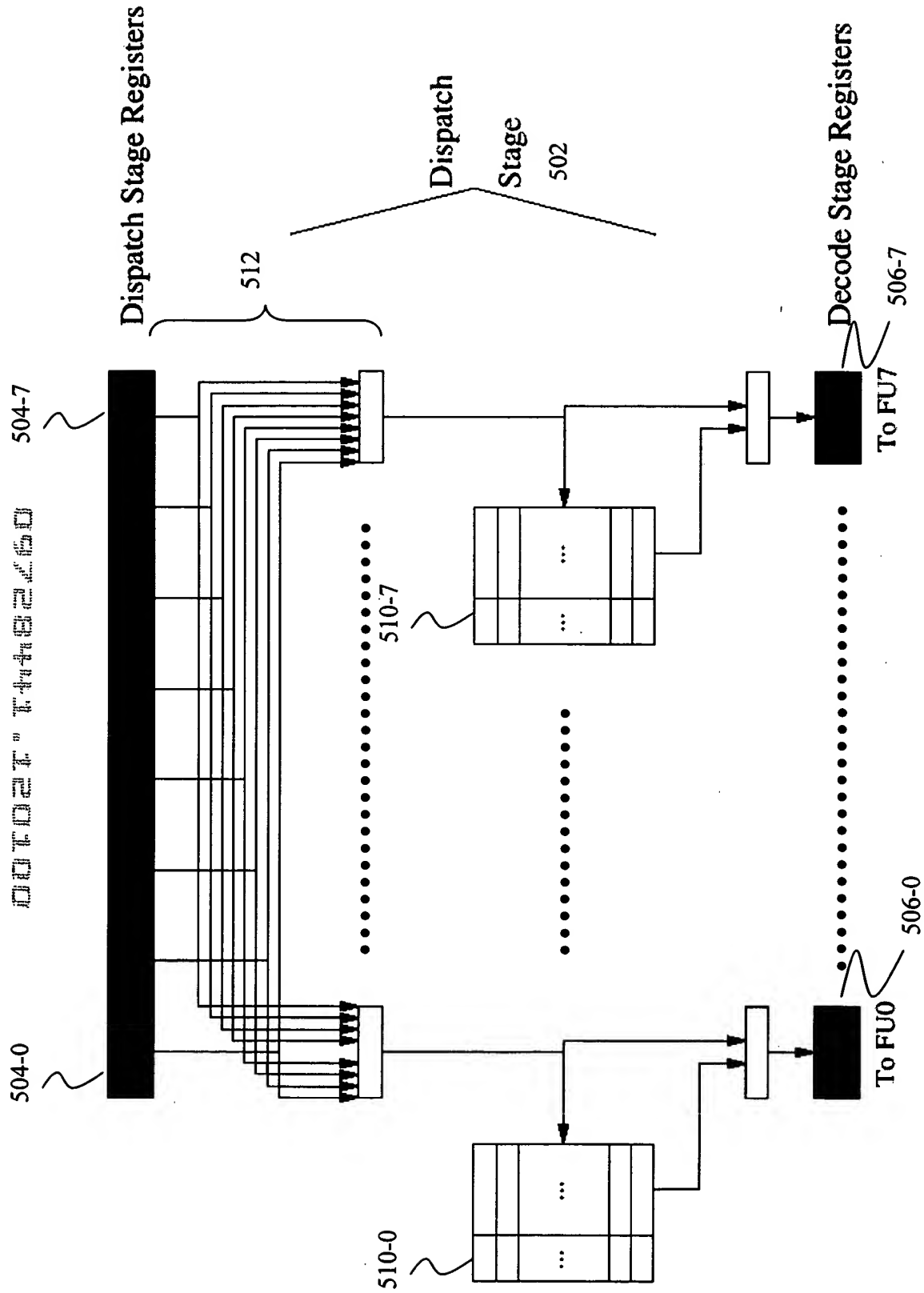


FIG. 5

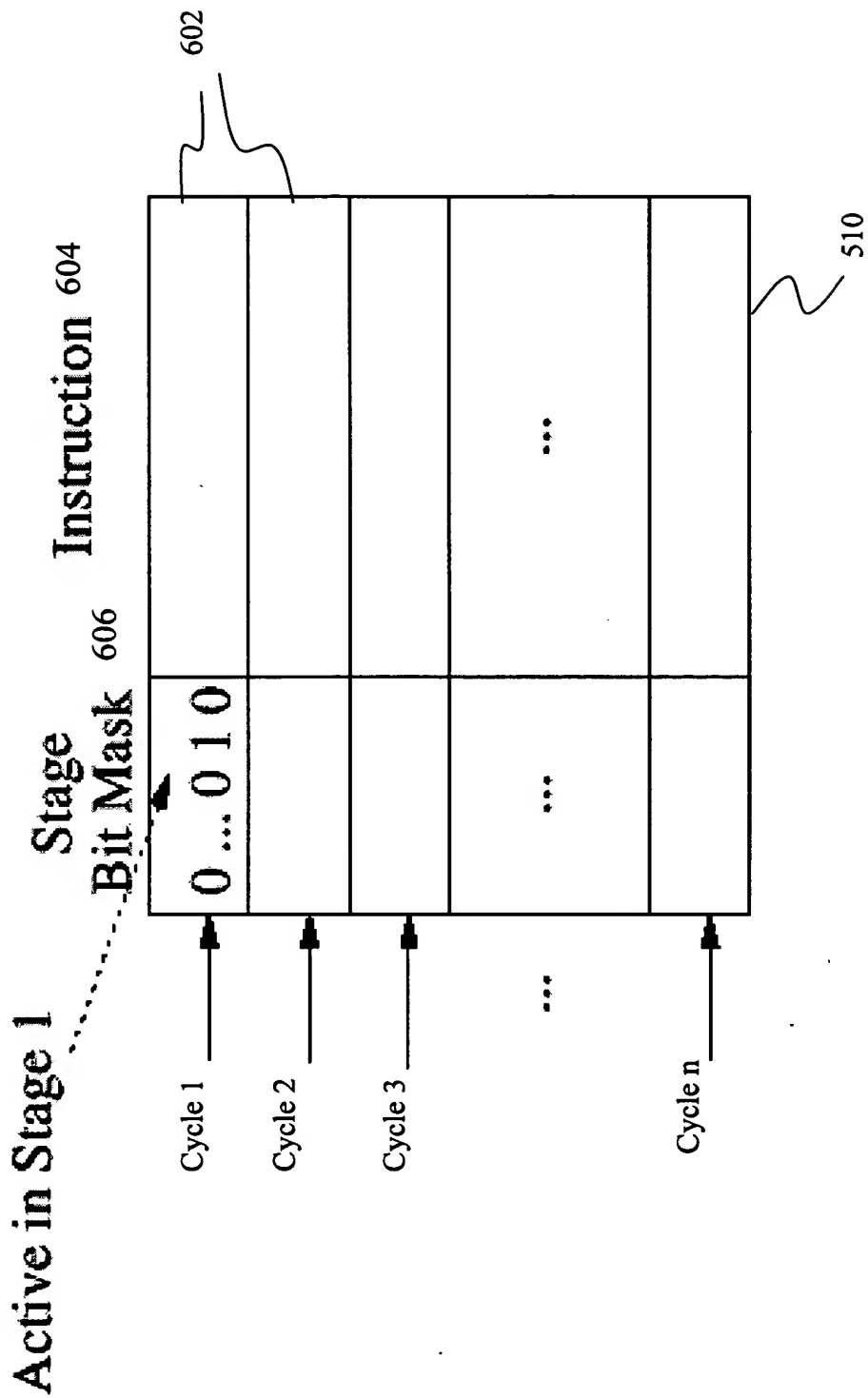


FIG. 6

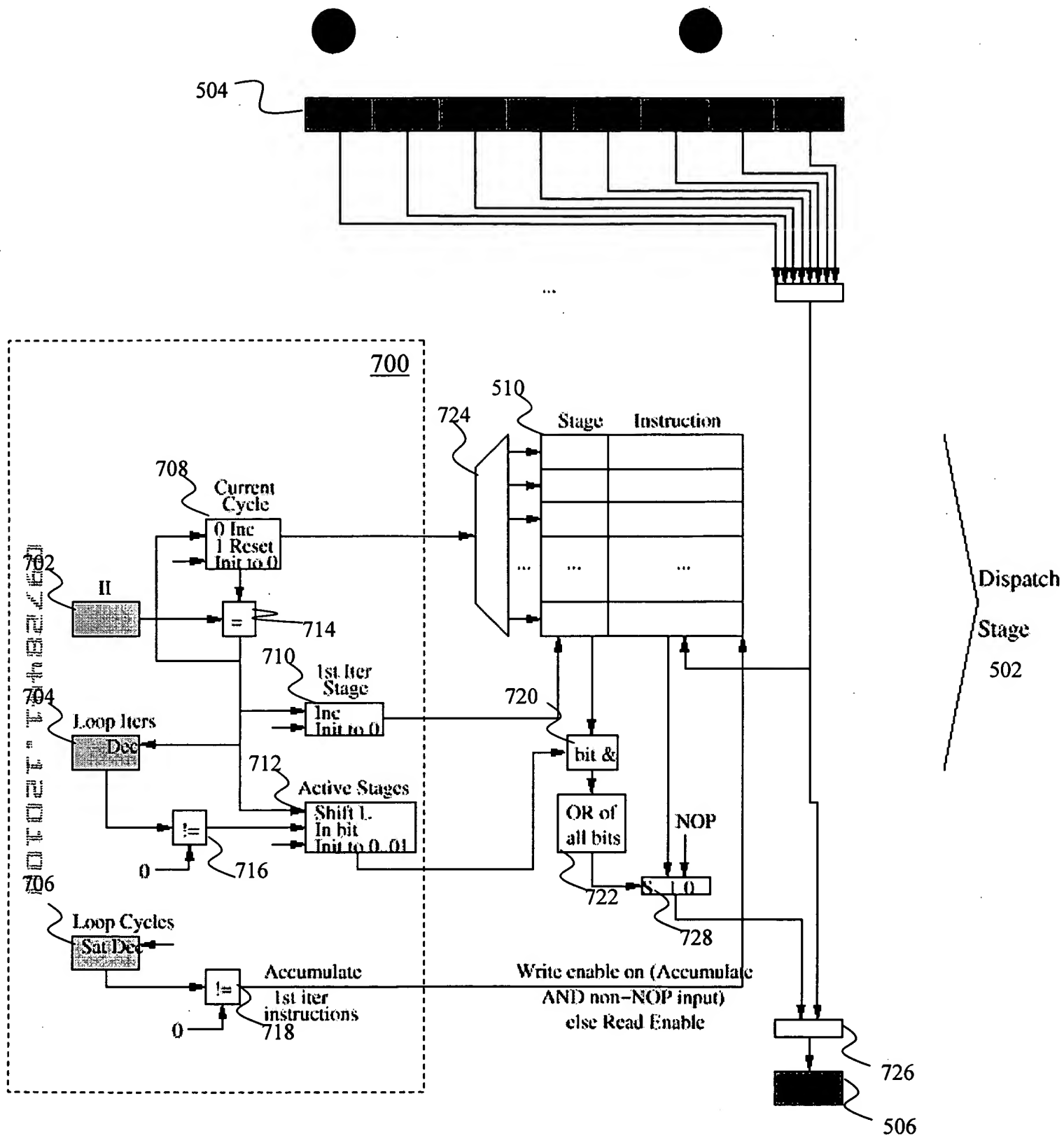


FIG. 7

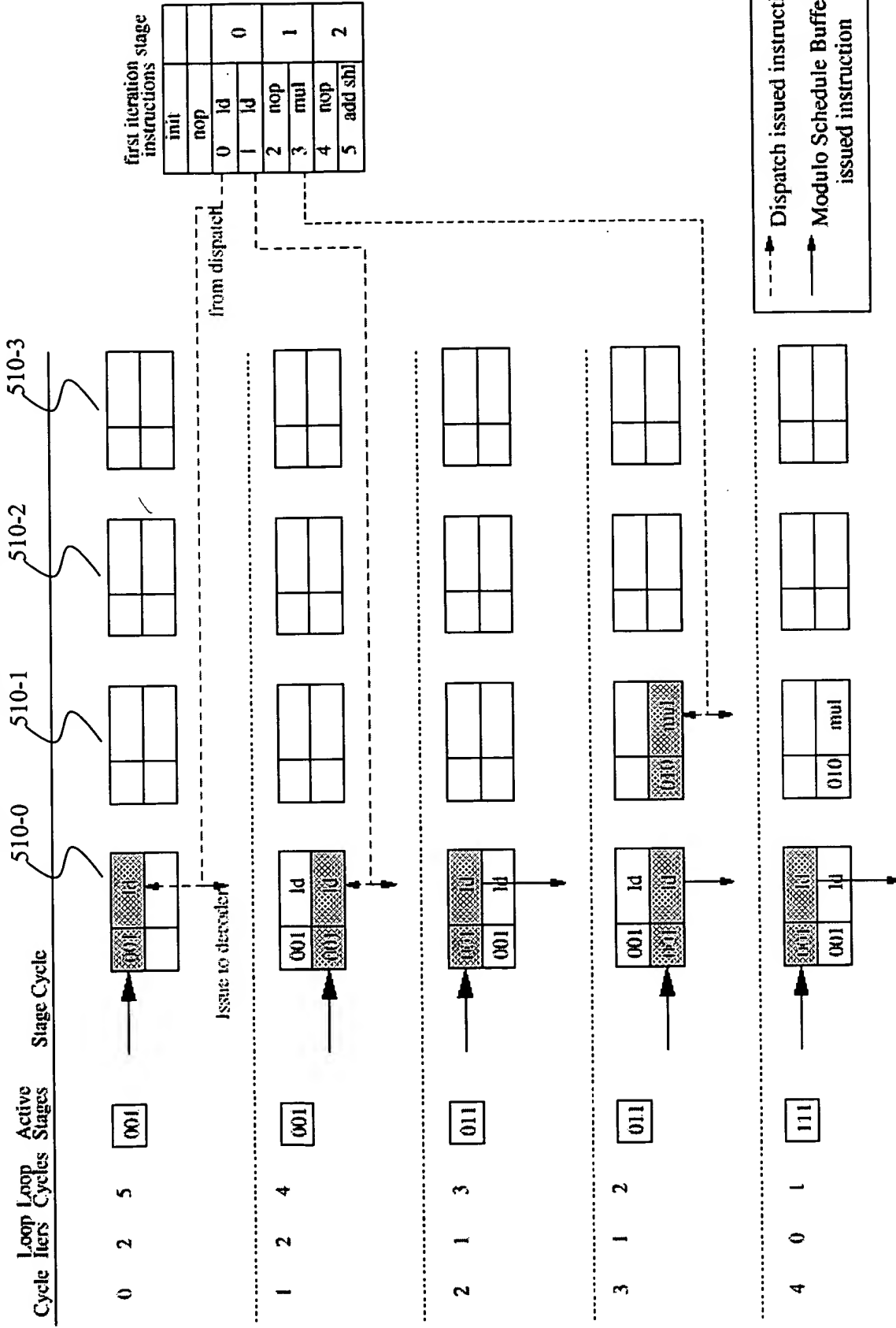


FIG. 8A

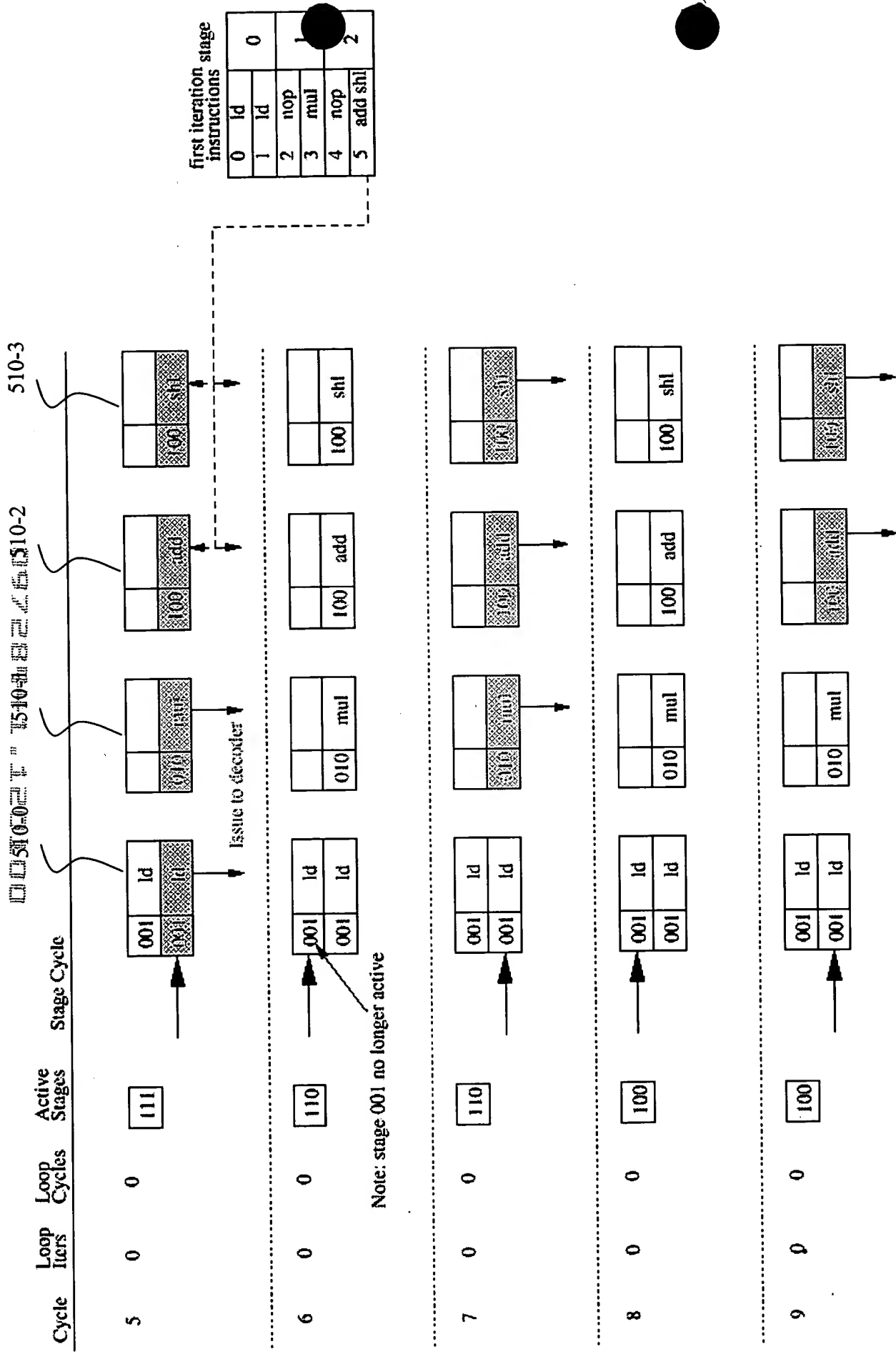


FIG 8B

cycle	RTL
0	$r1 \leftarrow 0$
1	$r1 \leftarrow r1 * 5$
2	$r1 \leftarrow r1 + 4$
3	$st[r2], r1$
4	$st[r3], r1$

inst.	latency
mul	3
add	1

FIG. 9

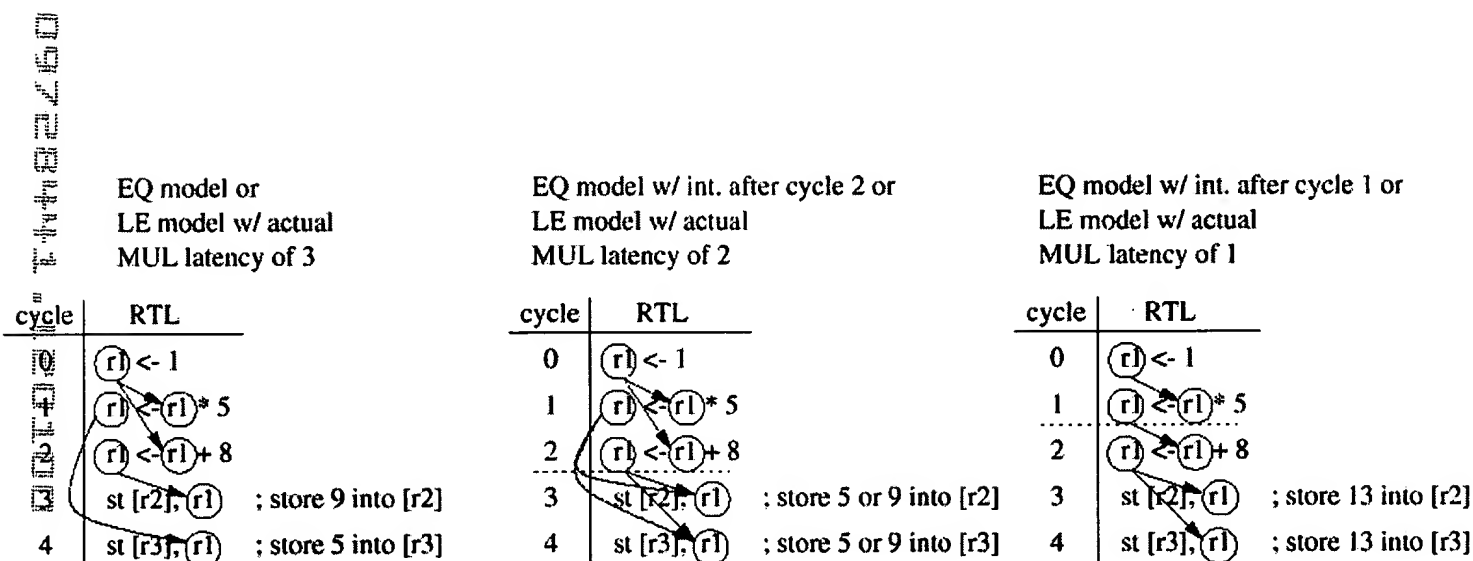


FIG. 10A

FIG. 10B

FIG. 10C

FIG. 11

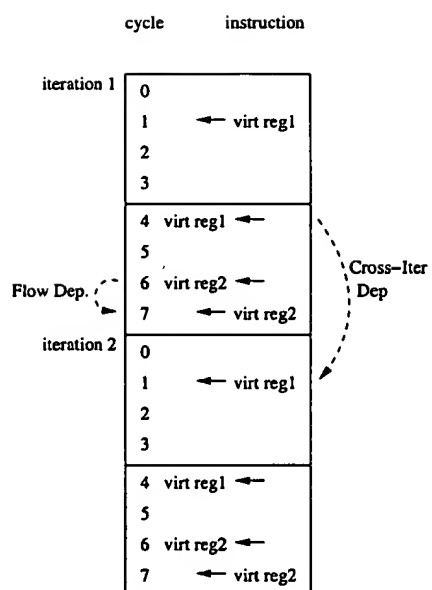
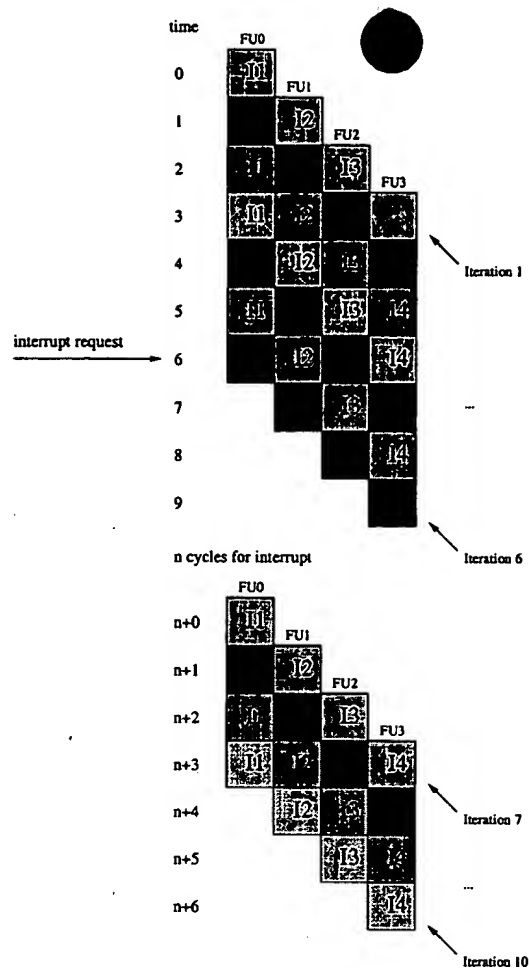


FIG. 12A

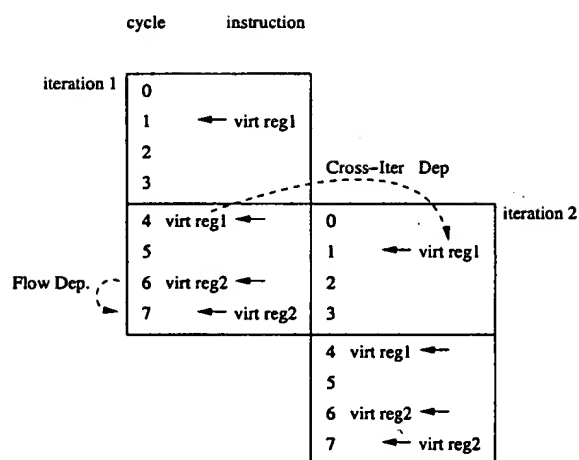


FIG. 12B

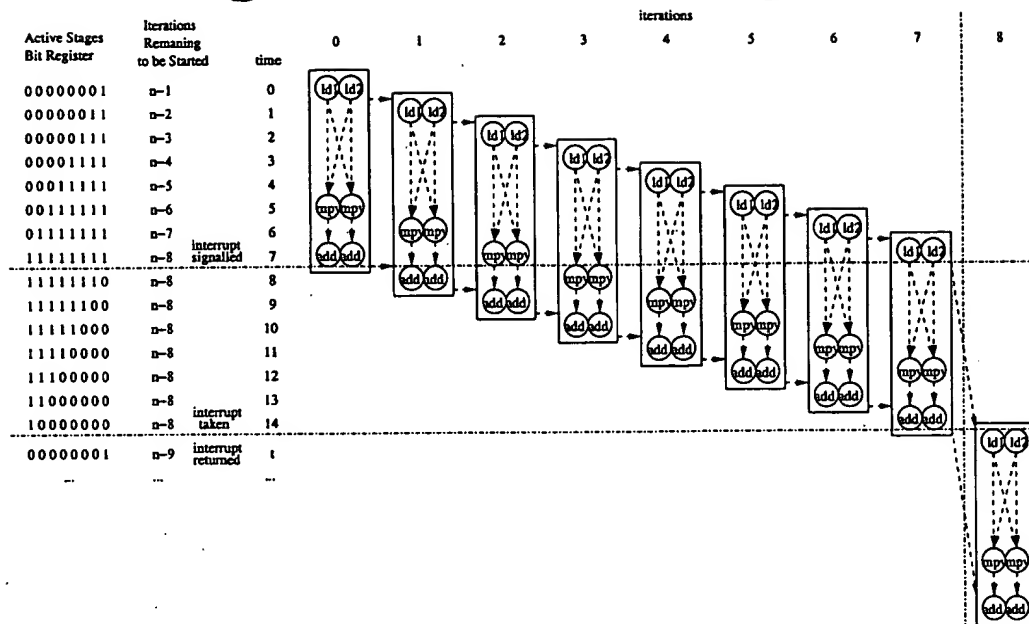


FIG. 13

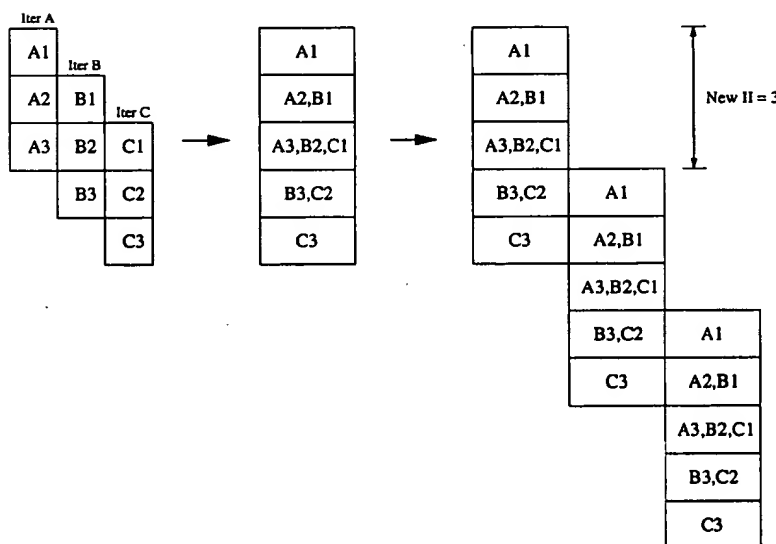


FIG. 14A

FIG. 14B

FIG. 14C